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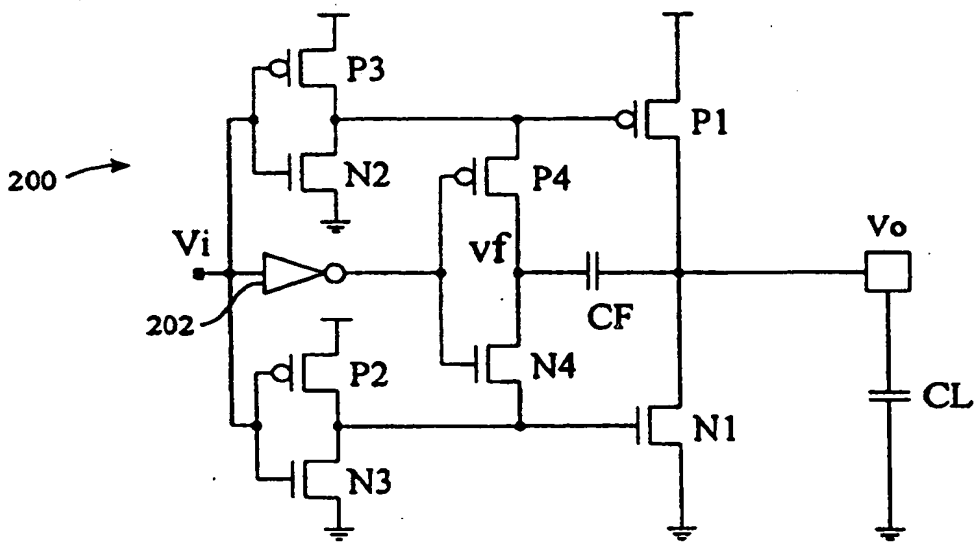

(57) Abstract

An output buffer (100; 200) in accordance with the present invention exhibits a fixed output signal slew rate. The output signal behavior is independent of the capacitive load (CL) seen by the buffer. The circuit includes a capacitive feedback path from the output node to circuitry which drives the output transistors. In one embodiment, the feedback path comprises two capacitive elements (CFP, CFN), one which comes into play during a rising edge transition and the other which affects a falling edge transition. In a second embodiment, a single capacitive element (CF) is coupled to a switching circuit (P4, N4) for use during either a falling transition or a rising transition. The second embodiment provides precharging of the output transistor gates, and so improves response time.

P-channel transistors P2 and P3 and N-channel transistors N2 and N3. Transistors P3 and N2 are coupled as an inverter I1, and transistors P2 and N3 are coupled as inverter I2.

The output of buffer 100 is driven by transistors P1 and N1, whose drains are coupled to output node v_o. The source of transistor P1 is coupled to V_{DD} while the source of transistor N1 is coupled to ground potential. The control gate of transistor P1 is coupled to the drains of transistors P3 and N2. Similarly, the control gate of transistor N1 is coupled to the drains of transistors P2 and N3.

Further in accordance with the present invention, a feedback path from output node v_o to the control gate of transistor P1 includes a capacitive element C_{FP}. Likewise, capacitive element C_{FN} is provided between output node v_o and the control gate of transistor N1. In the context of the present invention, a "capacitive element" is meant to refer to an actual capacitor device (e.g. devices C_{FN} and C_{FP}) which is to be distinguished from the parasitic capacitances inherently present in transistor devices. For example, Fig. 1 shows in phantom the parasitic gate capacitance C_{GN} for output transistor N1.

Still further in accordance with the present invention, for reasons which will become clear in the discussion below, transistor P3 is sized so that its W/L ratio is greater than that of transistor N2. In like manner, transistor N3 has a W/L ratio greater than that of transistor P2. The specific sizing of the devices depends upon the particular application. As an example, the transistor sizes used to generate the waveforms shown in the figures were: N1 = 120/0.8; P1 = 360/0.8; N2 = 2/24; P2 = 6/24; N3 = 10/0.8; and P3 = 30/0.8.

Turn now to a discussion of the operation of the circuit of Fig. 1. Consider the case of a falling transition of the input signal. At a time prior to such a transition, transistor P3 is OFF and transistor N2 is

in saturation and thus fully ON. Thus, output transistor P1 is fully ON and so load capacitor C_L is charged to V_{DD} potential. Similarly, transistor P2 is OFF and transistor N3 is ON, thus keeping output transistor N1 in the non-conducting OFF state.

Consider next the transition of the input signal to the lower voltage level. In such a situation, transistor N2 begins to turn OFF and transistor P3 begins to turn ON. Likewise, transistor N3 begins to turn OFF while transistor P2 begins to conduct. Recall that transistors P3, N2, N3, and P2 are sized so that P3 is stronger than N2 and N3 is stronger than P2; i.e. the W/L ratios of P3 and N3 are greater than N2 and P2 respectively. The consequence of such sizing is that the "inactive" output transistor (transistor P1 in the case of a falling transition) will turn OFF faster than the "active" output transistor (namely transistor N1) is turned ON. Conversely, in the case of a rising transition, the "inactive" output transistor N1 will turn OFF faster than the "active" output transistor P1 turns ON by virtue of N3 being stronger than P2. This is an important aspect of the invention, because such transistor sizing serves to eliminate a short circuit current between output transistors P1 and N1 during logic level transitions, thus isolating the circuitry which controls falling edge transitions from the circuitry which controls rising edge transitions.

The falling edge circuitry of output buffer 100 comprises: output transistor N1, feedback capacitor C_{FN}, transistor P2, parasitic capacitance C_{GN}, and output load capacitor C_L. These elements are shown in Fig. 2A. The waveform shown in Fig. 3 schematically illustrates three periods of time during the operation of the buffer for a falling edge transition.

Referring to Figs. 2B and 3, transistor N1 is OFF at the beginning of region A, and is shown in the equivalent circuit of Fig. 2B as a switch in the open position. Transistor P2 is in saturation and thus be-

haves like a constant current source, charging the parasitic gate capacitance C_{GN} of transistor N1 until node v_g reaches the threshold voltage of N1. In the meantime, since N1 is OFF, the increasing voltage at node v_g causes a corresponding increase in v_o through feedback capacitor C_{FN}. The time equations of the variation at node v_g and at the output node v_o can be determined.

The time function $v_g(t)$ for node v_g is:

$$v_g(t) = \frac{I}{C_1} \cdot t \qquad \text{Eqn. 1}$$

where C_1 is the total capacitance node v_g and I is the current provided by transistor P2

$$C_1 = C_{GN} + \frac{C_{FN} C_L}{C_{FN} + C_L}$$

The time function $v_o(t)$ for the output node is:

$$v_o(t) = V_{DD} + \frac{C_{FN}}{C_{FN} + C_L} \cdot v_g(t) \qquad \text{Eqn. 2}$$

Referring to Figs. 2C and 3, operation of the output buffer in region B and the corresponding equivalent circuit are shown. As P2 continues to charge capacitor C_{FN}, the gate voltage at node v_g continues to rise until output transistor N1 begins to turn ON. Consequently, the output load C_L begins to discharge through N1. At the same time, capacitor C_{FN} also begins to discharge through N1. This tends to slow the rising voltage at node v_g, which in turn reduces the current in N1. The rate at which C_{FN} discharges through N1 depends on the size of the load capacitance C_L.

C_{FN}, however, continues to be charged by transistor P2. This tends to raise the potential at node v_g,

and consequently the current in N1. This feedback effect will result in an equilibrium state where the discharge rate of capacitor C_{FN} through output transistor N1 is balanced by the charge rate of transistor P2. Thus at equilibrium, the voltage at node v_g (i.e. the gate voltage of transistor N1) remains constant during operation of the output buffer 100 in region B.

Since the gate voltage remains constant, output transistor N1 behaves like a constant current source, generating a constant output slope. The fall time for a falling edge transition therefore is perfectly controlled in this fashion.

As in the case of operation in region A, the equations for the voltage a node v_g and the time function $v_o(t)$ for output node v_o can be determined. The standard quadratic equation for modeling transistor activity in saturation is used for transistor N1, namely:

$$I_{N1} = \frac{K_{N1}}{2} \cdot (V_g - V_{TN1})^2 \qquad \text{Eqn. 3}$$

where:

K_{N1} is the transistor gain of N1
V_{TN1} is the threshold voltage of N1
I_{N1} is the current in N1

From which the constant gate voltage at node v_g is:

$$V_g = V_G = V_{TN1} + \sqrt{I_{N1} \frac{2}{K_{N1}}} \qquad \text{Eqn. 4}$$

At equilibrium, V_g is constant because N1 gate charging (by current I) is fully compensated by the discharge of the output load, leading to:

$$I = -C_{FN} \frac{dv_o}{d_t}$$

$$\frac{dv_o}{d_t} = -\frac{I}{C_{FN}} \qquad \text{Eqn. 5}$$

and the current in transistor N1 is:

$$I_{N1} = -(C_L + C_{FN}) \frac{dv_o}{d_t} \quad , \qquad \text{Eqn. 6}$$

Eqns. 5 and 6 can be used together to recast Eqn. 4 as:

$$I_{N1} = I \frac{C_L + C_{FN}}{C_{FN}}$$

$$V_G = V_{TN1} + \sqrt{\frac{2I}{K_{N1}} \cdot \frac{(C_L + C_{FN})}{C_{FN}}} \qquad \text{Eqn. 7}$$

The time varying function $v_o(t)$ for the output voltage is determined as follows:

$$I = -C_{FN} \frac{dv_o}{d_t} \qquad \text{Eqn. 8}$$

$$V_o(t) = V_{DD} + \frac{C_{FN}}{C_{FN} + C_L} \cdot V_G - \frac{I}{C_{FN}} (t - t_A)$$

where:

t_A is the duration of region A and is equal to $\frac{C1 \cdot V_G}{I}$, C_1 being taken from Eqn. 1;

V_G is the constant gate voltage expressed in Eqn. 7; and

the integration constant is $V_{DD} + \frac{C_{FN}}{C_{FN} + C_L} \cdot V_G$,

which takes into account the overshoot induced by the feedback capacitor during operation in region A.

The voltage V_G represents the control voltage to be applied to the output transistor N1 in order to discharge the output load C_L with a constant slope in a given time. It can be seen that the output slope is constant and depends only on internal elements, namely the charging current I provided by transistor P2 and the capacitance of feedback capacitor C_{FN}. The current I_{N1} through output transistor N1 during the discharge is adjusted to the load C_L, so that the slope of the output v_o is independent of the load.

Referring once again to Fig. 3, operation of the buffer in region C continues with the gate voltage at node v_g continuing to rise after the load capacitor is fully discharged. The gate of output transistor N1, therefore, will continue to rise until it reaches V_{DD} providing at that time full DC characteristics.

From the above equations, the propagation delay t_{PHL} and the fall time t_{SHL} can be deduced. The propagation delay is the sum of the delay in region A t_A and the delay necessary for the output to reach one-half of the supply voltage V_{DD}, thus:

$$t_{PHL} = \frac{C_{FN} + C_{GN}}{I} V_G + \frac{C_{FN}}{I} \frac{V_{DD}}{2} \qquad \text{Eqn. 9}$$

The fall time is measured between 90% and 10% of the output variation, thus:

$$t_{SHL} = \frac{C_{FN}}{I} \cdot 0.8V_{DD} \qquad \text{Eqn. 10}$$

Notice that in Eqn. 10, the fall time is independent of the output load C_L.

Turn now to the waveforms shown in Figs. 4A and 4B. These waveforms show the gate voltage measured at node v_g and the output voltage measured at output node v_o.

Waveforms are generated for varying output loads: 10 pF, 30 pF, 100 pF, and 300 pF; for an output buffer in accordance with the present invention shown in Fig. 4A and for a classic output buffer shown in Fig. 4B. Fig. 4A also identifies the three regions A - C of operation initially shown in Fig. 3.

Consider first Fig. 4A. The effect of the feedback capacitor is shown in region B where the gate voltage is flat. As a result of the constant gate voltage, the slew rate of the signal at the output node v_o is constant for all capacitive loads. The effects of the load capacitance do not come into play until the device is operating in region B. As shown in Fig. 4A, the load capacitance C_L determines the time it takes for the charging and discharging of feedback capacitor C_{FN} to reach equilibrium, as evidenced by the onset of the flat portion of the V_g waveforms.

By comparison, the waveform shown in Fig. 4B of a classic buffer without the feedback capacitor shows that the gate voltage reaches V_{DD} almost instantaneously, thus putting output transistor N1 immediately into saturation. Consequently, with transistor N1 at maximum conductivity, the discharge rate at the output node v_o is a function of the time constant defined by the load capacitance C_L and the channel resistance of N1. The slew rate therefore will vary with the capacitive load, since the channel resistance remains constant.

Fig. 5A shows that output buffer 100 produces a constant drain current in transistor N1 during operation in region B, the current self-adjusts to different levels depending on the load C_L. Because of this self-adjusting behavior, the discharge time is the same regardless of the size of the load. A larger load having a greater charge stored, will discharge more current in a given amount of time, while a smaller load having a smaller charge stored will discharge less current in that same amount of time. The result is a constant slew rate regardless of load capacitance. In contrast, the drain

current profile of a classic output buffer shown in Fig. 5B indicates that the load discharges at the maximum rate, the time for discharge simply being a function of the amount of charge stored in the load. The result is a slew rate that varies depending on the load capacitance.

As a final observation, the propagation delay of the present invention is increased by a factor of about eight, as can be seen by comparing the output waveforms in Figs. 4A and 4B. Referring to Figs. 5A and 5B, the circuit of the present invention shows a reduced current peak by the same factor. The reduced current peak helps to minimize noise. As can be seen in Fig. 5A, the current reducing capability is even better for smaller loads.

The foregoing discussion addresses the operation of the output buffer during a falling transition, and so focuses on the bottom half of the buffer circuitry 100 depicted in Fig. 1. A similar analytical treatment is possible with respect to a rising transition which involves the upper half of the buffer circuitry. It can be shown that for a rising transition, the slope of the changing voltage at output node v_o is the same regardless of the capacitive load C_L.

Turn now to Fig. 6 for a discussion of a second embodiment of the invention. Transistors P1 - P3 and N1 - N3 are the same as those comprising output buffer 100 in Fig. 1. The embodiment shown in Fig. 6 includes an inverter 202 whose input is coupled to input node v_i. Transistor P4 has a first terminal coupled to the control gate of output transistor P1 and a second terminal coupled to node v_f. Transistor N4 has a first terminal coupled to the control gate of output transistor N1 and a second terminal coupled to node v_f. The gates of transistors P4 and N4 are tied together and coupled to the output of inverter 202. A feedback capacitor C_F is coupled between output node v_o and node v_f. As will be discussed below, transistors P4 and N4 serve as a switching element to selectively couple one end of feedback capacitor C_F

either to the control gate of output transistor P1 or the control gate of output transistor N1.

Operation of the circuit 200 shown in Fig. 6 is similar to the circuit of Fig. 1 in all respects, except for the following aspect. Consider a falling transition. The conditions just prior to the transition are: the potential at input node v_i is V_{DD}. Thus, transistors N2, N3, and P4 are turned ON, while transistors P3, P2, and N4 are OFF. Consequently, the gate voltage of output transistor P1 is held at zero by transistor N2, and the gate voltage of output transistor N1 is held at zero by transistor N3. P1 is therefore ON and output node v_o is held at V_{DD}.

The output of inverter 202 is zero, thus turning ON transistor P4 and turning OFF transistor N4. Observe that although P4 is ON, the potential at node v_f cannot rise above $-V_{tP4}$, the threshold voltage of P4. The reason is that, under these conditions, node v_f is the source node for P4. Recall that conduction occurs when $V_{gs} >= V_t$. In this case, $V_{gs} = 0 - V_f$, where V_f is the potential at node v_f. When V_f reaches $-V_{tP4}$, any tendency for node v_f to rise above $-V_{tP4}$ will turn OFF P4. V_f, therefore, stabilizes at $-V_{tP4}$. Similarly, it can be shown that in a rising transition scenario V_f will not rise above $(V_{DD} - V_{tN4})$.

When the transition occurs, transistor N4 turns ON, thus transferring the charge at feedback capacitor C_F to the gate of output transistor N1 through a process known as charge sharing. Thus, the gate of N1 can be precharged to a level close to its threshold voltage by appropriately sizing the feedback capacitor C_F.

In accordance with the invention, N4 is fully turned ON prior to transistor P2 turning ON. This is accomplished by sizing the P-channel and N-channel transistors of inverter 202 so that they are faster than P3/N2 and P2/N3. Thus, during a falling transition, inverter 202 will go high before transistor P2 turns ON, and during a rising transition, the inverter will go low

before transistor N2 turns ON. This provides a quick precharge of the gate of N1 (or P1 in the case of a rising transition) before the transistor P2 (N2) turns ON and begins charging the gate. By precharging the gate, the output load C_L can begin to discharge at an earlier time during the transition as compared to the buffer circuit of Fig. 1. Consequently, the propagation delay is reduced. The gain on the propagation delay due to the precharging is equal to the delay necessary, with the circuit of Fig. 1, for the gate voltage to reach the precharge voltage. Considering that the value of the feedback capacitor C_F is negligible against the value of the output load C_L, the following expression for the propagation delay is obtained:

$$t_{PHL} = \frac{C_F + C_L}{I} V_G + \frac{C_F}{I} \cdot \left(\frac{V_{DD}}{2} - |V_t| \right) \qquad \text{Eqn. 11}$$

where:

Vt is the threshold voltage of transistor P4 in the case of falling transitions, and N4 in the case of rising transitions.

In addition, overshoots are also reduced because of the precharging by feedback capacitor C_F. The precharging eliminates the charge build-up at the output that occurs with the circuit of Fig. 1 as the gate capacitance is being charged during operation in region A (Fig. 3). With precharging, there is effectively no region A.

This is shown in Fig. 7A where it can be seen that the gate voltage instantly reaches the threshold voltage of the output transistor (P1, N1) due to precharging by the feedback capacitor. Thus, the onset of the falling edge occurs at a time earlier than in the circuit of Fig. 1, and so propagation delay is reduced.

Note that precharging also has eliminated the overshoot that exists at the onset of the falling transition in the circuit of Fig. 1. The drain current profiles of Fig. 7B also show the increased responsiveness of output buffer 200 as compared to the profile of Fig. 5A for output buffer 100.

Another aspect of the embodiment of Fig. 6 is the reduced area of the circuitry on silicon. Note that the circuit of Fig. 6 uses one feedback capacitor C_F as compared to the circuit of Fig. 1 which uses two feedback capacitors C_{FN}, C_{FP}. Capacitors consume a large area as compared to transistors. For example, a 1 pF capacitor is roughly 25 x 55 μM in area. Thus, while the circuit of Fig. 6 uses more transistors than does the circuit of Fig. 1, the total area required of the former circuit is still smaller than that of the latter circuit because of the use of only one capacitor. Typical W/L ratios for transistors N4, P4 are 8/0.8 μM and 24/0.8 μM respectively. Similarly, the transistors comprising inverter 202, are also small; e.g. 4/0.8 μM for the N-channel device and 12/0.8 μM for the P-channel device are deemed sufficient for driving the small gate capacitances of transistors N4 and P4.

Claims

1. An output buffer circuit comprising:

a signal-receiving node (Vi);

a first inverter (P3,N2) having input and output terminals, the input terminal coupled to the signal-receiving node;

a second inverter (P2,N3) having input and output terminals, the input terminal coupled to the signal-receiving node;

a first output transistor (P1) having first and second terminals and having a gate terminal coupled to the output terminal of the first inverter;

a second output transistor (N1) having first and second terminals and having a gate terminal coupled to the output terminal of the second inverter;

a signal output node (Vo) to which the second terminal of the first output transistor and the first terminal of the second output transistor are coupled; and

a capacitive feedback means (CFP,CFN;CF) for coupling the signal output node back to the gate terminals of the first and second output transistors.

2. The output buffer circuit of claim 1 wherein the capacitive feedback means includes a first capacitive element (CFP) coupled between the signal output node and the gate terminal of the first output transistor (P1) and a second capacitive element (CFN) coupled between the signal output and the gate terminal of the second output transistor (N1).

3. The output buffer circuit of claim 2 wherein the first output transistor (P1) is a P-channel device and the second output transistor (N1) is an N-channel device.

4. The output buffer circuit of claim 1 wherein the capacitive feedback means further includes third and fourth transistors (P4,N4) coupled in series and connected between the gates of the first and second output transistors, and a third inverter (202) coupled between the signal-receiving node and gates of the third and fourth transistors.

5. The output buffer circuit of claim 4 wherein the first output transistor (P1) is a P-channel device and the second output transistor (N1) is an N-channel device.

6. The output buffer circuit of claim 5 wherein the third transistor (P4) is a P-channel device and the fourth transistor (N4) is an N-channel device.

7. The output buffer circuit of claim 1 wherein the first inverter includes a P-channel device (P3) and an N-channel device (N2), the P-channel device having a greater W/L ratio than the N-channel device.

8. The output buffer circuit of claim 7 wherein the second inverter includes a P-channel device (P2) and an N-channel device (N3), the N-channel device having a greater W/L ratio than the P-channel device.

9. An output buffer circuit comprising:

an input node (Vi) and an output node (Vo);

an input stage having first and second inverters (P3,N2;P2,N3), each inverter having an input coupled to the input node;

a P-channel transistor (P1) having a gate terminal coupled to an output of the first inverter and further having a drain terminal coupled to the output node (Vo);

an N-channel transistor (N1) having a gate terminal coupled to an output of the second inverter and further having a drain terminal coupled to the output node (Vo);

a first capacitive element (CFP) coupled between the drain and gate terminals of the P-channel transistor; and

a second capacitive element (CFN) coupled between the drain and gate terminals of the N-channel transistor.

10. The output buffer circuit of claim 9 wherein the first inverter includes a P-channel device and an N-channel device, the P-channel device having a greater width dimension than the N-channel device.

11. The output buffer circuit of claim 9 wherein the second inverter includes a P-channel device and an N-channel device, the N-channel device having a greater width dimension than the P-channel device.

12. An output buffer comprising:

a signal input node (Vi);

a signal output node (Vo);

a first inverter (P3,N2) having an input terminal coupled to the signal input node and further having an output terminal;

a pull-up transistor (P1) having a first terminal for being coupled to a first potential, a second terminal coupled to the signal output node, and a control terminal coupled to the output terminal of the first inverter;

a second inverter (P2,N3) having an input terminal coupled to the signal input node and further having an output terminal;

a pull-down transistor (N1) having a first terminal for being coupled to a second potential, a second terminal coupled to the signal output node, and a control terminal coupled to the output terminal of the second inverter; and

a capacitive feedback path having a capacitive element (CF) and switching means (P4,N4,202), the capacitive element having a first end coupled to the signal output node, the switching means for selectively coupling a second end of the capacitive element between the control gate of the pull-up transistor and the control gate of the pull-down transistor.

13. The output buffer of claim 12 wherein the switching means includes a third inverter (202), a P-channel transistor (P4), and an N-channel transistor (N4); the third inverter having an input terminal coupled to the signal input node (Vi) and further having an output terminal coupled to control gates of the P-channel and N-channel transistors; the transistors having a common drain connection; a source of the P-channel transistor coupled to the control gate of the pull-up transistor (P1); a source of the N-channel transistor coupled to the control gate of the pull-down transistor (N1); the common drain connection being coupled to the second end of the capacitive element (CF).

14. The output buffer circuit of claim 12 wherein the first inverter includes a P-channel device (P3) and an N-channel device (N2), the P-channel device having a greater W/L ratio than the N-channel device.

15. The output buffer circuit of claim 14 wherein the second inverter includes a P-channel device (P2) and an N-channel device, the N-channel device (N3) having a greater W/L ratio than the P-channel device.

AMENDED CLAIMS

[received by the International Bureau on 19 March 1999 (19.03.99); original claims 2-4 and 9-11 cancelled; original claims 1 and 12 amended; remaining claims unchanged (3 pages)]

1. An output buffer circuit comprising:

a signal-receiving node (Vi);

a first inverter (P3,N2) having input and output terminals, the input terminal coupled to the signal-receiving node;

a second inverter (P2,N3) having input and output terminals, the input terminal coupled to the signal-receiving node;

a first output transistor (P1) having first and second terminals and having a gate terminal coupled to the output terminal of the first inverter;

a second output transistor (N1) having first and second terminals and having a gate terminal coupled to the output terminal of the second inverter;

a signal output node (Vo) to which the second terminal of the first output transistor and the first terminal of the second output transistor are coupled; and

a capacitive feedback means (CF) for coupling the signal output node back to the gate terminals of the first and second output transistors, including third and fourth transistors (P4,N4) coupled in series and connected between the gates of the first and second output transistor and a third inverter (202) coupled between the signal-receiving node and gates of the third and fourth transistors.

2. Canceled

3. Canceled

4. Canceled

5. The output buffer circuit of claim 4 wherein the first output transistor (P1) is a P-channel device and the second output transistor (N1) is an N-channel device.

6. The output buffer circuit of claim 5 wherein the third transistor (P4) is a P-channel device and the fourth transistor (N4) is an N-channel device.

7. The output buffer circuit of claim 1 wherein the first inverter includes a P-channel device (P3) and an N-channel device (N2); the P-channel device having a greater W/L ratio than the N-channel device.

8. The output buffer circuit of claim 7 wherein the second inverter includes a P-channel device (P2) and an N-channel device (N3), the N-channel device having a greater W/L ratio than the P-channel device.

9. Canceled

10. Canceled

11. Canceled

12. An output buffer comprising:

a signal input node (Vi);

a signal output node (Vo);

a first inverter (P3,N2) having an input terminal coupled to the signal input node and further having an output terminal;

a pull-up transistor (P1) having a first terminal for being coupled to a first potential, a second terminal coupled to the signal output node, and a control terminal coupled to the output terminal of the first inverter;

a second inverter (P2,N3) having an input terminal coupled to the signal input node and further having an output terminal;

a pull-down transistor (N1) having a first terminal for being coupled to a second potential, a

second terminal coupled to the signal output node, and a control terminal coupled to the output terminal of the second inverter; and

a capacitive feedback path having a capacitive element (CF) and switching means (P4,N4,202), the capacitive element having a first end coupled to the signal output node, the switching means for selectively coupling a second end of the capacitive element directly to either the control gate of the pull-up transistor the control gate of the pull-down transistor.

13. The output buffer of claim 12 wherein the switching means includes a third inverter (202), a P-channel transistor (P4), and an N-channel transistor (N4); the third inverter having an input terminal coupled to the signal input node (Vi) and further having an output terminal coupled to control gates of the P-channel and N-channel transistors; the transistors having a common drain connection; a source of the P-channel transistor coupled to the control gate of the pull-up transistor (P1); a source of the N-channel transistor coupled to the control gate of the pull-down transistor (N1); the common drain connection being coupled to the second end of the capacitive element (CF).

14. The output buffer circuit of claim 12 wherein the first inverter includes a P-channel device (P3) and an N-channel device (N2), the P-channel device having a greater W/L ratio than the N-channel device.

15. The output buffer circuit of claim 14 wherein the second inverter includes a P-channel device (P2) and an N-channel device, the N-channel device (N3) having a gr ater W/L ratio than the P-channel device.

STATEMENT UNDER ARTICLE 19

The invention is directed to an output buffer circuit having an input node and an output node, with first and second inverters having inputs coupled to the input node. Outputs of the inverters are coupled to the gates of first and second drive transistors. The drive transistors have a common drain connection coupled to the output node. A capacitive feedback path includes series coupled third and fourth transistors having a common gate connection and a common drain connection. A capacitor is coupled between the common drain and the output node. An inverter is coupled between the input node and the common gate.

The reference to Boomer shows in Figs. 2 and 3 an output buffer having a capacitive feedback path comprising a first capacitor (Cp) coupled between the output node (Vout) and the gate of a first drive transistor (P1) and a second capacitor (Cn) coupled between the output node and the gate of a second drive transistor (N1). No other capacitive feedback paths are shown.

The reference to Lewis shows in Fig. 4 an output buffer having a first capacitor (Cin) coupled between the gate of a first drive transistor (20) and ground and a second capacitor (Cip) coupled between the gate of a second drive transistor (22) and ground. The Lewis reference does not disclose the use of any capacitive feedback paths.

The reference to Nessi et al. is directed to a slew rate controlled output driver for use with switched inductive loads. The circuitry disclosed avoids the immediate and abrupt transfer of charge that characterizes switched circuits. Figure 3 shows a circuit which avoids such changes in current. The circuit includes a pair of integrating stages (op-amps, unnumbered) which share a capacitor (cu). The capacitor is switched (s1, s2) between the op-amps. Signals (NW, PW) operate each switch in synchrony so that capacitor (cu) is coupled to only one op-amp at a time. The slew rates during the turn-off phase of the output transistors (PU, NU) are controlled to avoid abrupt changes by an integrating effect during operation of the integrating stages.

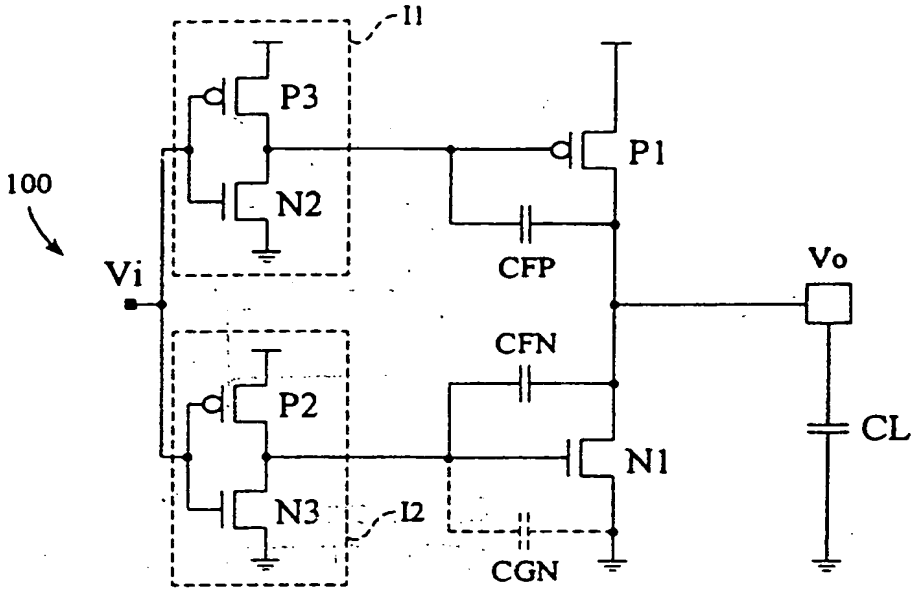
100
Vi
P3
N2
I1
P1
CFP
Vo
CFN
P2
N3
I2
N1
CGN
CL

Fig. 1

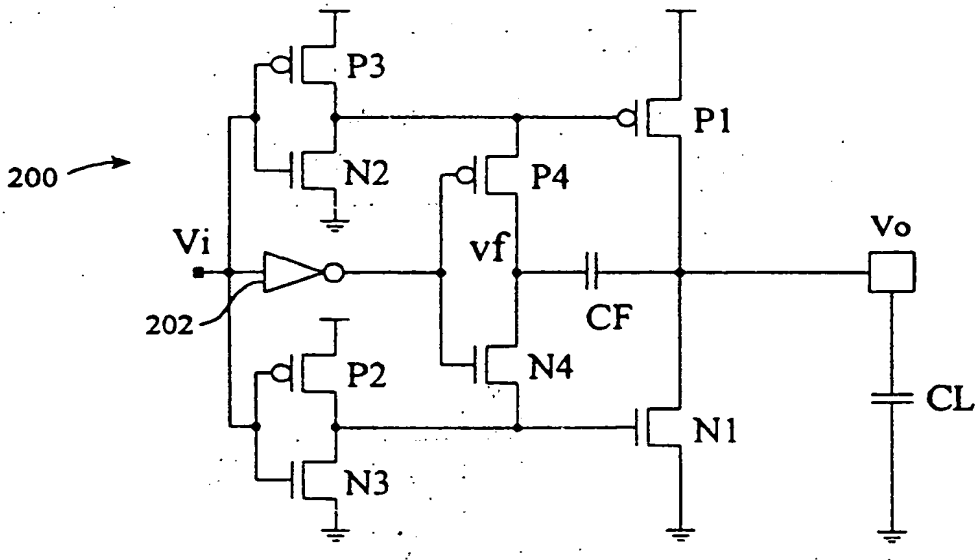
200
Vi
202
P3
N2
P4
vf
P1
CF
Vo
P2
N4
N1
N3
CL

Fig. 6

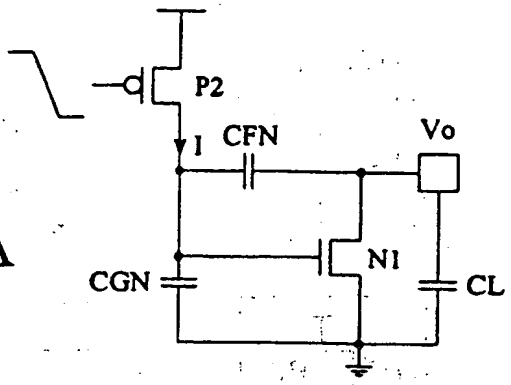

Fig. 2A

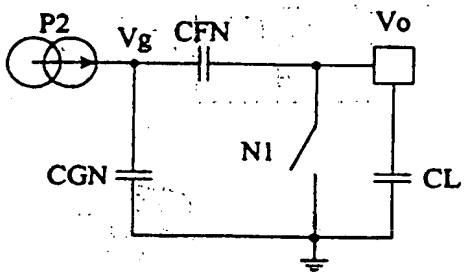

Fig. 2B

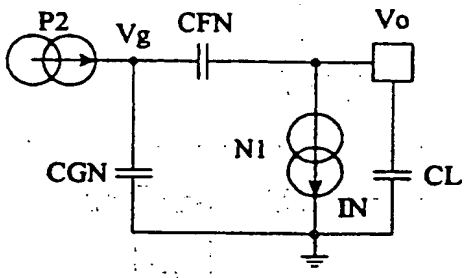

Fig. 2C

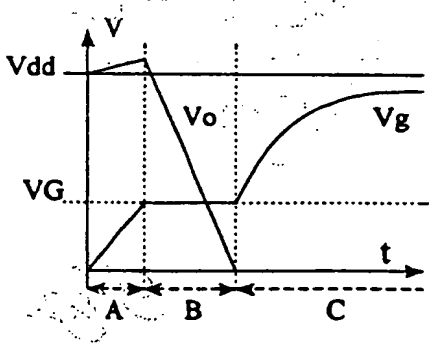

Fig. 3

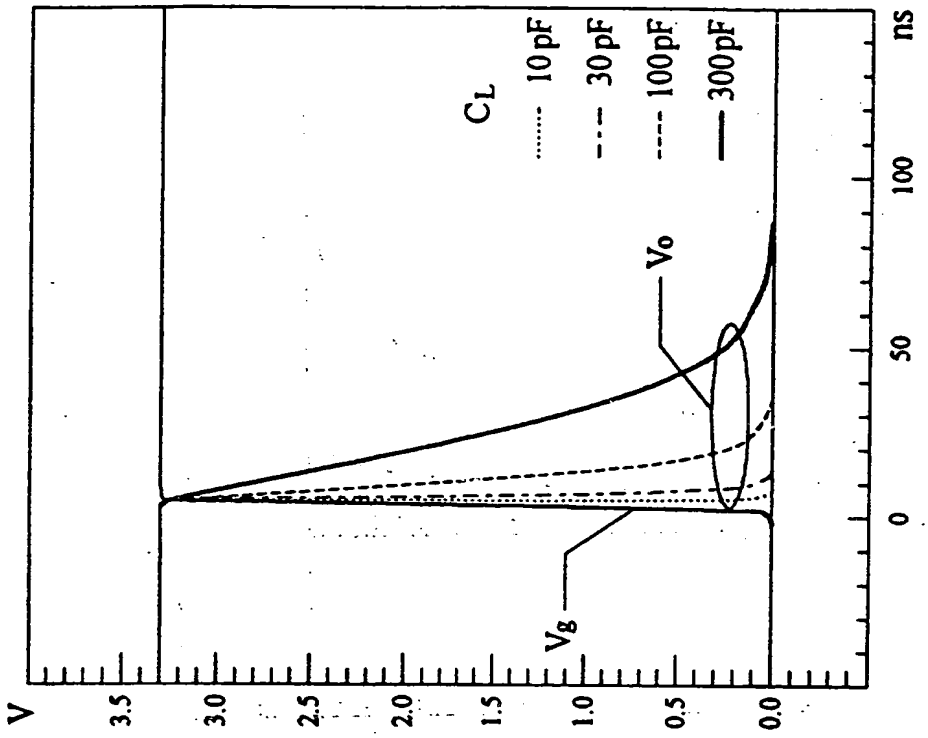

Fig. 4B

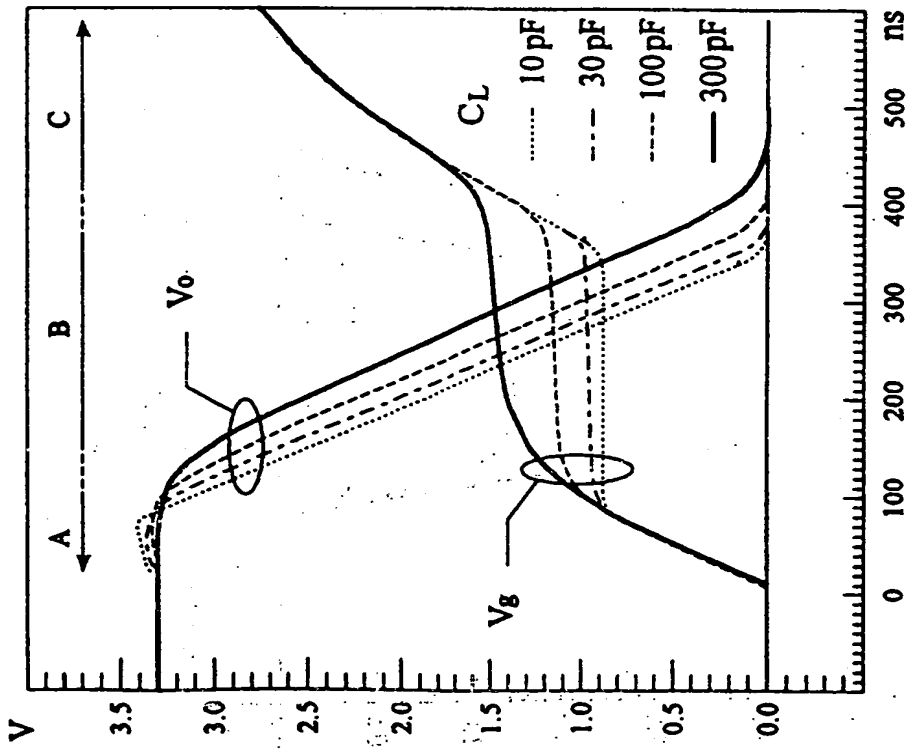

Fig. 4A

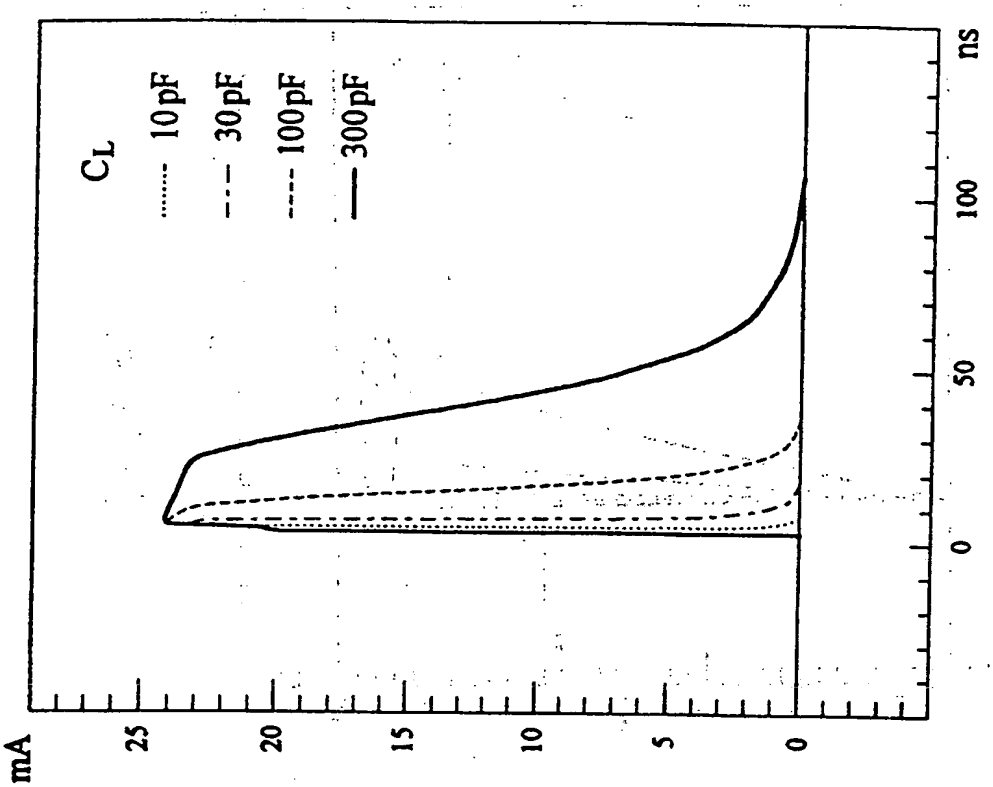

Fig. 5B

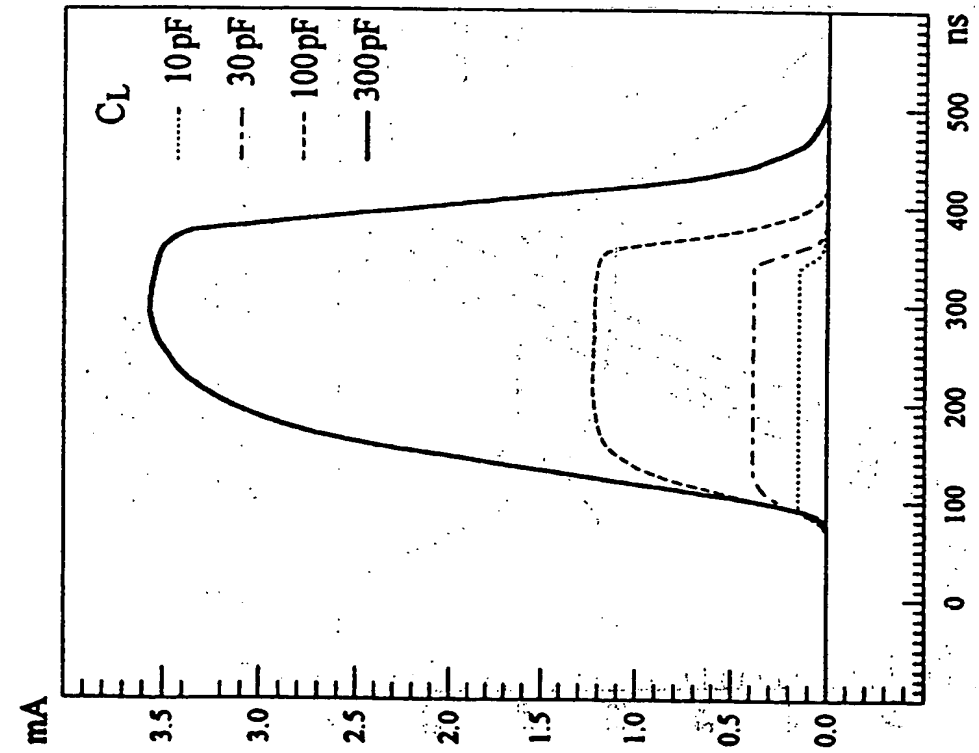

Fig. 5A

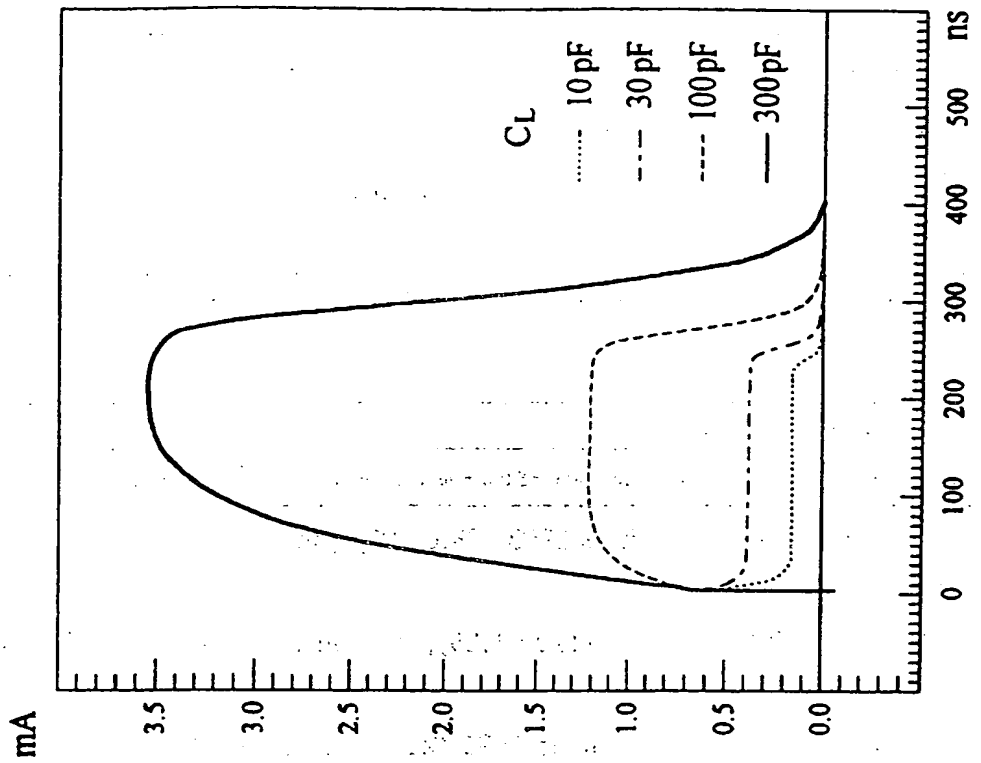

Fig. 7B

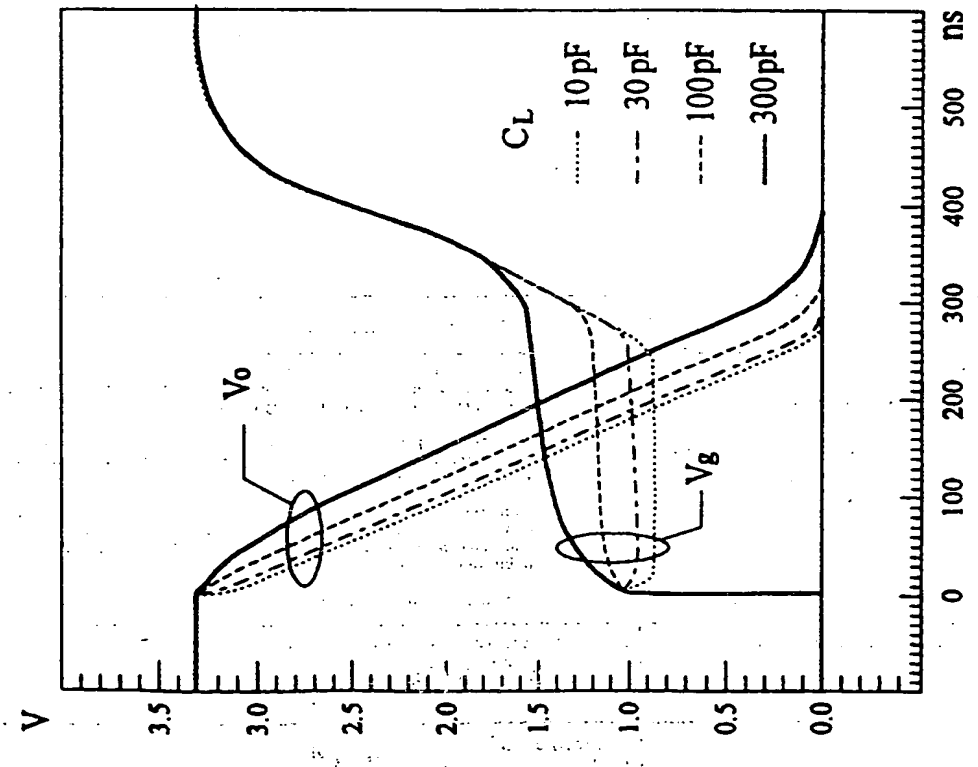

Fig. 7A

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/24394

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03K 3/00; HO3B 1/00

US CL :326/26, 27; 327/108, 111, 112, 379, 390

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/26, 27, 87, 88; 327/108, 109, 110, 111, 112, 379, 382, 389, 390

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,218,239 X (BOOMER et al) 08 June 1993 (08.06.93) (figure 3)	1-3, 9
X	US 4,797,579 X (LEWIS) 10 January 1989 (10.01.89), see figure 4.	7-8, 10-11, and 14-15
X	US 5,469,096 X (NESSI et al) 21 November 1995 (21.11.95) see figure 3.	12-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
19 FEBRUARY 1999	26 FEB 1999

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	DAN T. LUU
Facsimile No. (703) 305-3230	Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet)(July 1992)★